Built-In Self Test Method and Apparatus for Jitter Transfer, Jitter Tolerance, and FIFO Data Buffer

ABSTRACT OF THE DISCLOSURE

Testing a transceiver includes providing a sequence of test signals. A serialization clock is generated and jitter is added to the clock in a known and controlled manner. The test signals can then be transmitted using the serialization clock. After the test signals are recovered by the clock and data recovery mechanism, the recovered sequence is compared to the original sequence, to test for jitter tolerance. Preferably, each of these steps is performed on chip. In other aspects, a jitter transfer test and/or a FIFO test can be performed.